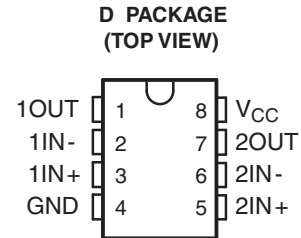


FEATURES

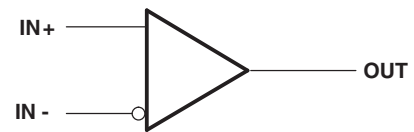
- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 100 V Using Machine Model (C = 200 pF, R = 0)**
- **Single or Dual-Supply Operation**
- **Wide Range of Supply Voltages . . .4 V to 18 V**
- **Very Low Supply Current Drain . . .150 μ A Typ at 5 V**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Built-in ESD Protection**
- **High Input Impedance . . . $10^{12}\Omega$ Typ**
- **Extremely Low Input Bias Current. . .5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μ V/Month, Including the First 30 Days**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Common-Mode Input Voltage Range Includes Ground**
- **Output Compatible With TTL, MOS, and CMOS**
- **Pin-Compatible With LM393**



SYMBOL (each comparator)



DESCRIPTION/ORDERING INFORMATION

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 4 V to 18 V. Each device features extremely high input impedance (typically greater than $10^{12}\Omega$), allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships.

The TLC372 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating using human-body-model (HBM) testing. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC372 is characterized for operation from –55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

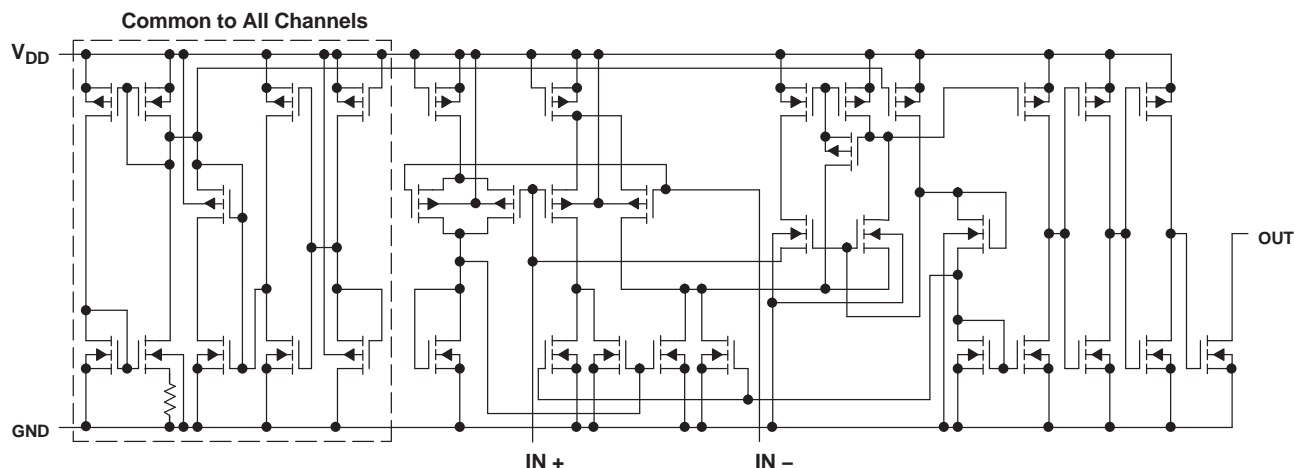
LinCMOS is a trademark of Texas Instruments.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC-(D)	Tape and reel	TLC372MDREP	372MEP

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
 (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

EQUIVALENT SCHEMATIC (EACH COMPARATOR)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V _{DD} Supply voltage ⁽²⁾		18	V
V _{ID} Differential input voltage ⁽³⁾		±18	V
V _I Input voltage range	–0.3	18	V
V _O Output voltage		18	V
I _I Input current		±5	mA
I _O Output current		20	mA
Duration of output short circuit to ground ⁽⁴⁾	unlimited		
Continuous total power dissipation	See Dissipation Rating Table		
T _A Operating free-air temperature range	–55	125	°C
T _{stg} Storage temperature range	–65	150	°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s:		260	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 (2) All voltage values except differential voltages are with respect to network ground.
 (3) Differential voltages are at IN+ with respect to IN–.
 (4) Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

Dissipation Rating Table

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR	DERATE ABOVE T _A	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	145 mW

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Supply voltage		4	16	V
V_{IC}	Common-mode input voltage	$V_{DD} = 5\text{ V}$	0	3.5	V
		$V_{DD} = 10\text{ V}$	0	8.5	
T_A	Operating free-air temperature		-55	125	°C

Electrical Characteristics

at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICRmin}^{(2)}$		25°C		1	5	mV
				Full range			10	
I_{IO}	Input offset current			25°C		1		pA
				Max			10	nA
I_{IB}	Input bias current			25°C		5		pA
				Max			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD} - 1$			V
				Full range	0 to $V_{DD} - 1.5$			
I_{OH}	High-level output current	$V_{ID} = 1\text{ V}$	$V_{OH} = 5\text{ V}$	25°C	0.1			nA
			$V_{OH} = 15\text{ V}$	Full range			3	μA
V_{OL}	Low-level output voltage	$V_{ID} = -1\text{ V}$,	$I_{OL} = 4\text{ mA}$	25°C		150	400	mV
				Full range			700	
I_{OL}	Low-level output current	$V_{ID} = -1\text{ V}$,	$V_{OL} = 1.5\text{ V}$	25°C	6	16		mA
I_{DD}	Supply current (two comparators)	$V_{ID} = 1\text{ V}$,	No load	25°C		150	300	μA
				Full range			400	

(1) All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is -55°C to 125°C. IMPORTANT: See Parameter Measurement Information.

(2) The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD} . They can be verified by applying the limit value to the input and checking for the appropriate output state.

Switching Characteristics

$V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, $C_L = 15\text{ pF}^{(1)(2)}$	100-mV input step with 5-mV overdrive	650	ns
		TTL-level input step	200	

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC372 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

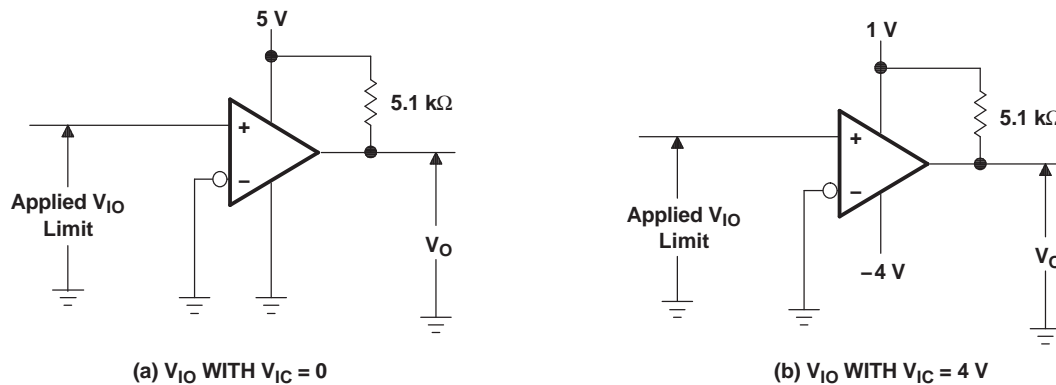


Figure 1. Method for Verifying That Input Offset Voltage is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

PARAMETER MEASUREMENT INFORMATION (continued)

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

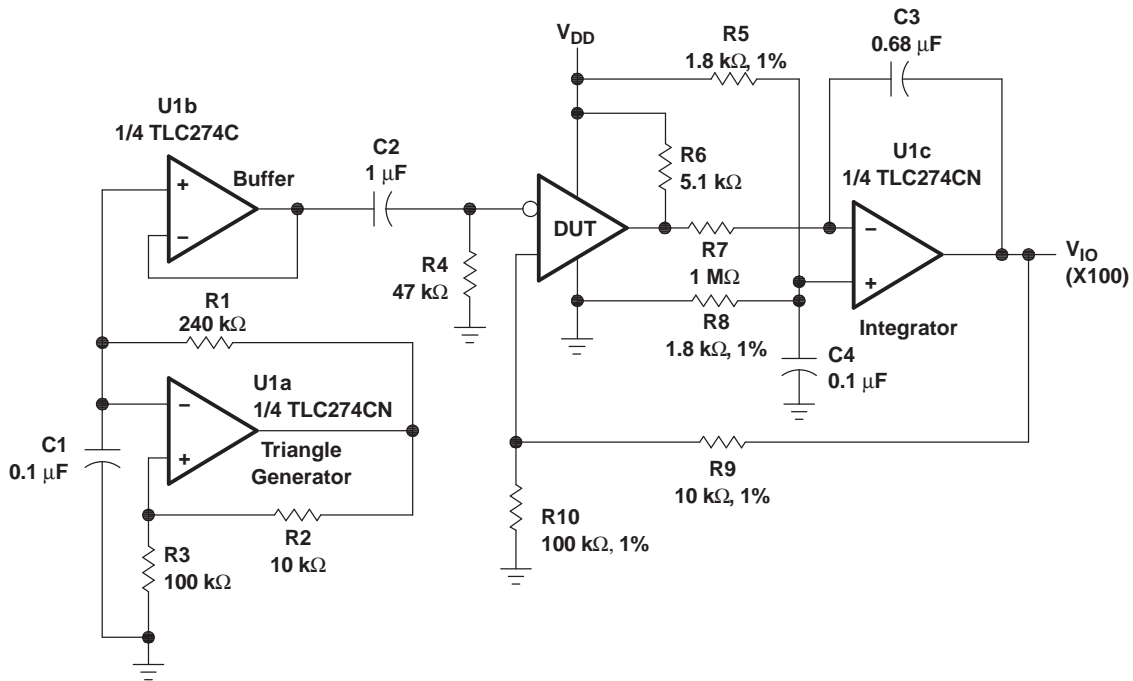


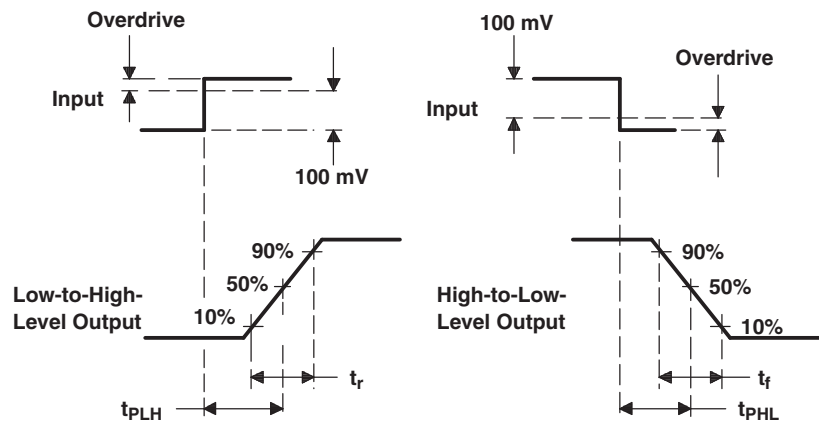
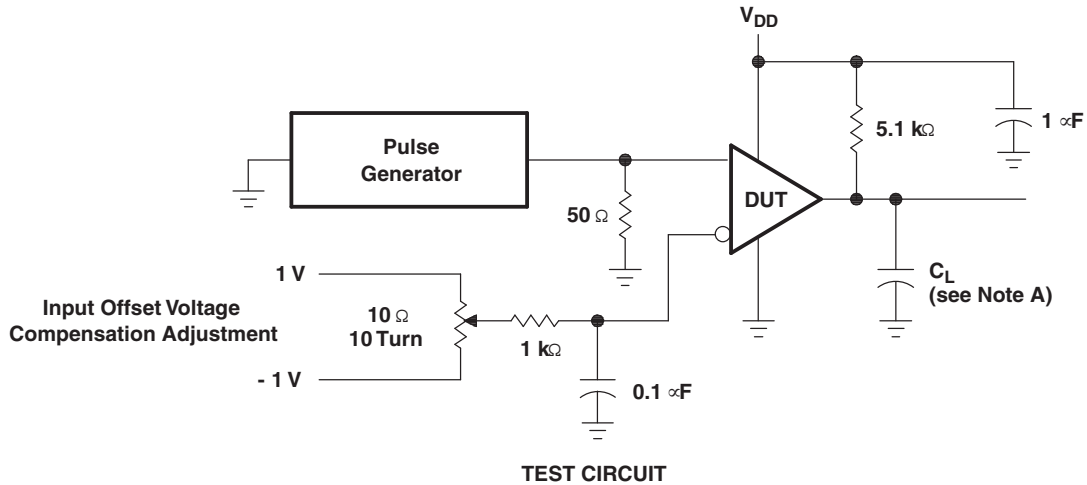
Figure 2. Circuit for Input Offset Voltage Measurement

Voltage divider R9 and R10 provides a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION (continued)

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 3, so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.



NOTE: A. C_L includes probe and jig capacitance

Figure 3. Response, Rise, and Fall Times Circuit and Voltage Waveforms

PRINCIPLES OF OPERATION

LinCMOS™ Process

The LinCMOS process is a linear polysilicon-gate complementary-MOS process. Primarily designed for single-supply applications, LinCMOS products facilitate the design of a wide range of high-performance analog functions, from operational amplifiers to complex mixed-mode converters.

This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS products. Further questions should be directed to the nearest TI field sales office.

Electrostatic Discharge (ESD)

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. ESD is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g. during board assembly. If a circuit in which one amplifier from a dual operational amplifier is being used and the unused pins are left open, high voltages tends to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in [Figure 4](#). This circuit can withstand several successive 1-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of TI's ESD-protection circuit is presented in Circuit Design Consideration.

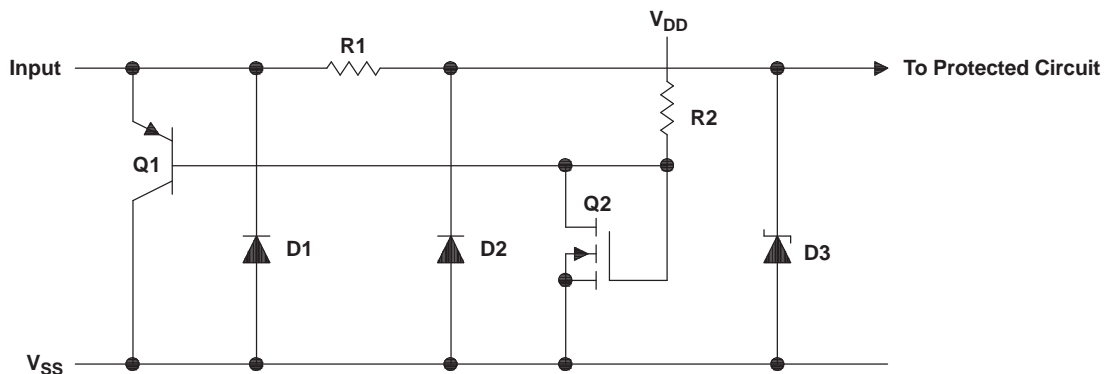


Figure 4. LinCMOS™ ESD-Protection Schematic

Input Protection Circuit Operation

Texas Instruments patented protection circuitry allows for both positive-and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

PRINCIPLES OF OPERATION (continued)

Positive ESD Transients

Initial positive charged energy is shunted through Q1 to V_{SS} . Q1 turns on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{EB} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level ($V_T \sim 22\text{ V to } 26\text{ V}$) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the n-channel enhancement-type MOSFET Q2 to V_{SS} . If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded, and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 V to 27 V, which is well below the gate oxide voltage of the circuit to be protected.

Negative ESD Transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is $-0.3\text{ V to } -1\text{ V}$ (the forward voltage of D1 and D2).

Circuit-Design Considerations

LinCMOS products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is $\pm 5\text{ mA}$. [Figure 5](#) and [Figure 6](#) show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limits the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in [Figure 5](#). This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see [Figure 7](#)).

PRINCIPLES OF OPERATION (continued)

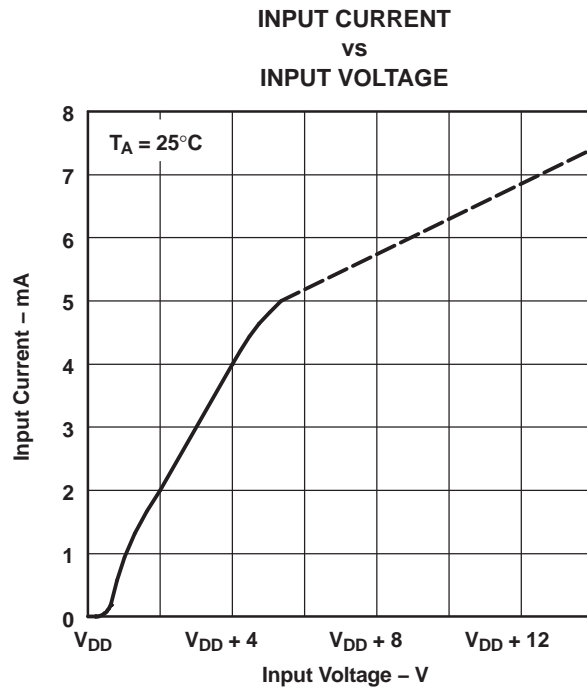


Figure 5.

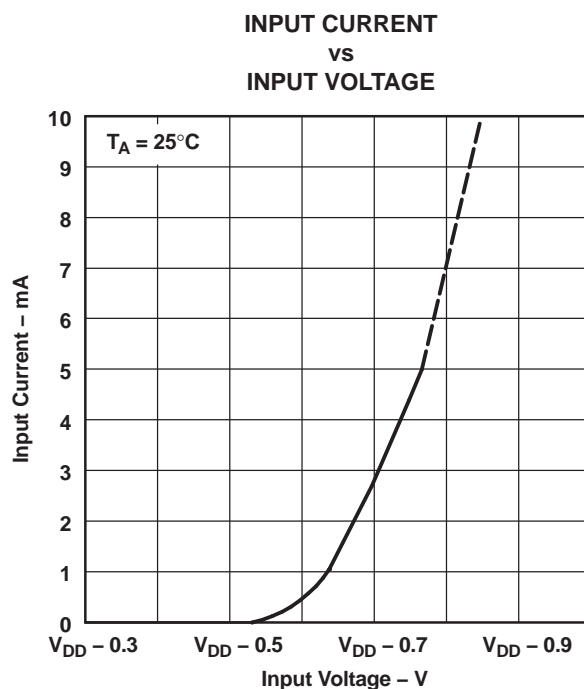
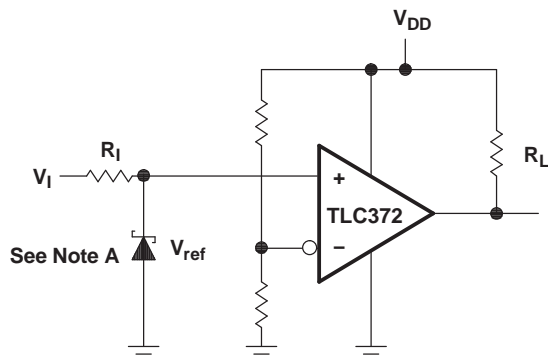


Figure 6.

PRINCIPLES OF OPERATION (continued)



Positive Voltage Input Current Limit:

$$R_I = \frac{+V_I - V_{DD} - 0.3 \text{ V}}{5 \text{ mA}}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{DD} - (-0.3 \text{ V})}{5 \text{ mA}}$$

- A. If the correct output state is required when the negative input exceeds V_{SS} , a Schottky clamp is required.

Figure 7. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLC372MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06675-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF TLC372-EP :

- Catalog: [TLC372](#)
- Military: [TLC372M](#)

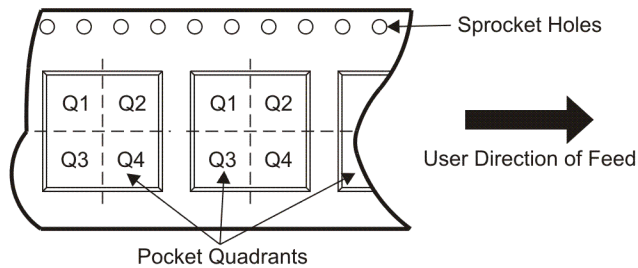
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC372MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

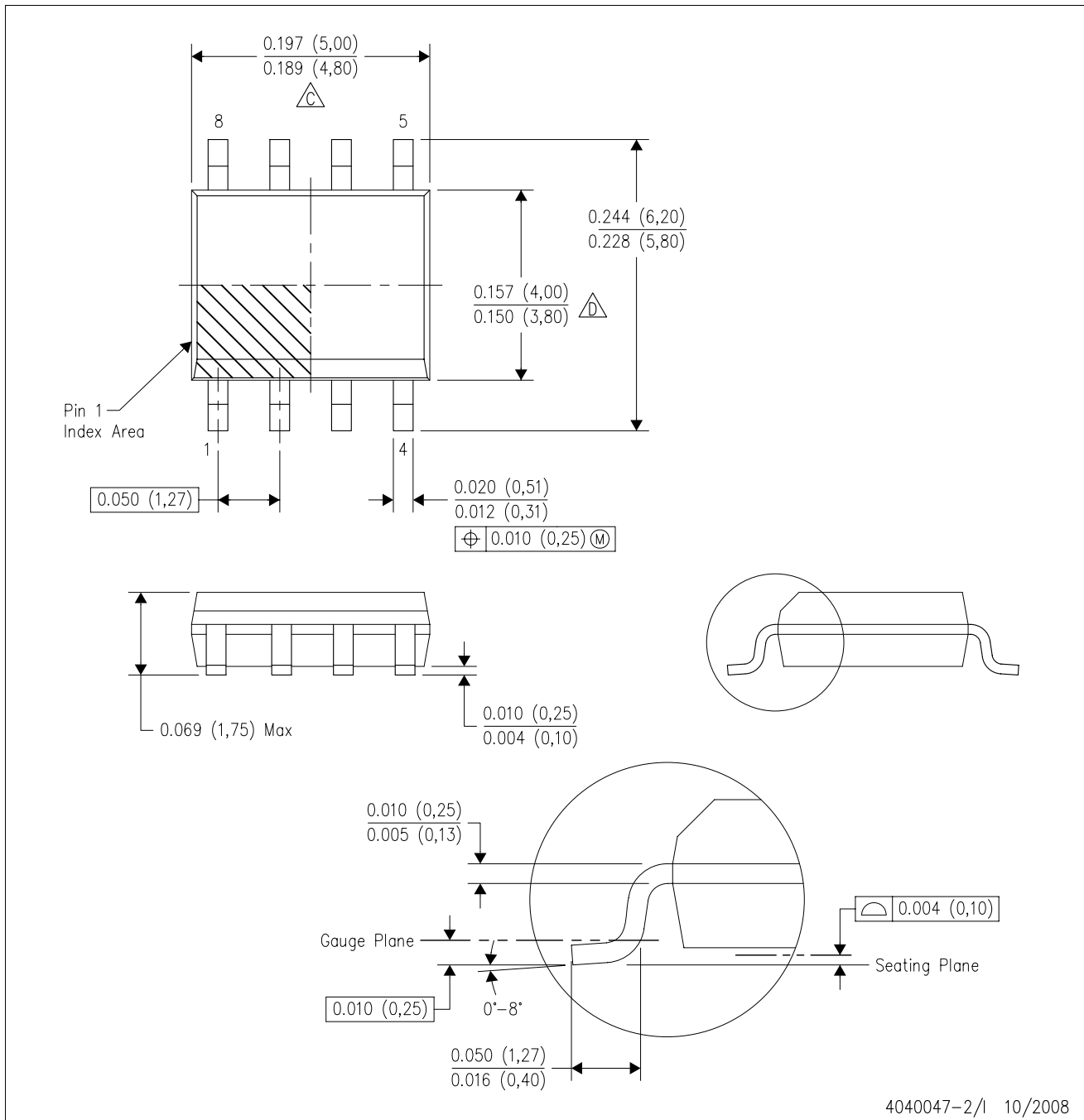




*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC372MDREP	SOIC	D	8	2500	346.0	346.0	29.0

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

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